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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/633,213

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Thane Michael Larson

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12/01/2006

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EXAMINER

ALPHONSE, FRITZ

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 12/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/633,213

Applicant(s)

LARSON ET AL.

Examiner

Fritz Alphonse

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2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-10 and 13-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 4-10, 13-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

0.1 This office action is in response to amendment filed on 9/01/2006. Claims 1 and 10 are amended.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 4-10, 13-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig (U.S. Pat. No. 6,038,680) in view of Berney (U.S. Pat. No. 6,299,068) and further in view of MacLaren (US Pub. No. 20020016942).

As to claim 10, Olarig (figs. 1- 4) shows an apparatus to visually locate a memory module (55) in a memory system (37) with a plurality of memory modules (col. 2, lines 37-47), the apparatus comprising: a system board (see figure 4; col. 3, lines 26-45; col. 5, lines 32-47) including a memory controller (29) and a plurality of memory module slots (54) on the system board (i.e., motherboard 53, 57); and a plurality of memory modules seated in the plurality of memory module slots (fig. 4; col. 5, lines 48-55); and a beacon unit (i.e., registers 58) on a memory module with a beacon device and control circuitry for turning on the beacon device when an electronic communication to turn on the beacon device is received by that memory module (col. 6, lines 1-18).

Olarig differs from claim 10 in that he does not teach "the beacon device comprises an electromechanical device that remains activated even in the absence of

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power.” However, the limitation is obvious and very well known in the art, as evidenced by Berney (see col. 29, lines 41-45).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention to combine Olarig’s system with the opto-electronic device, as disclosed by Berney. Doing so would provide highly reliable communication links among signals even after complete loss of power, and acknowledgements of all alarm and control messages.

In addition, as to claim 10, Olarig and Berney do not specifically disclose a device which visibly shows the beacon state when activated.

However, in the same field of endeavor, MacLaren discloses a system for detecting data errors in a memory device including a light emitting diode (LED) which visibly shows a beacon state (illuminate an LED) when activated (paragraph [0056]).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time of the invention to improve upon the hard/soft error detection device, as disclosed by MacLaren. Doing so would provide early error detection which may reduce the occurrences of uncorrectable errors and prevent future system failures.

As to claims 13-15, Olarig discloses an apparatus, wherein the memory modules comprise dual in-line memory modules (DIMMs); and, wherein the memory modules comprise single in-line memory modules (SIMMs). See column 5, lines 33-47.

As to claims 16-21, Olarig discloses an apparatus, wherein the system board comprises a computer motherboard; the system board comprises a cell board. Olarig (fig. 5) discloses an apparatus, further comprising a memory error interface unit (72) on the

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system board that is configured to send the appropriate electronic communication to the memory module (col. 5, lines 33-47).

As to claims 22-26, Olarig discloses an apparatus, wherein the beacon unit (i.e., registers 58) further comprises a second beacon device and control circuitry for turning on the second beacon device. The beacon device and the second beacon device are of different colors to visually distinguish them (col. 6, lines 1-18).

As to claim 27, Olarig (figs. 1- 4) shows a system for visually locating a memory module, the system comprising: means for receiving an electronic communication by circuitry on the memory module to be visually located (col. 2, lines 20-28); means for activating a beacon state in the memory module due to receipt of the electronic communication (col. 6, lines 1-18); and means for electronically turning on a beacon device on the memory module when the beacon state is activated to draw attention to that memory module (col. 5, lines 49-54; col. 7, lines 59 through col. 8 line 3).

As to claim 1, method claim 1 corresponds to apparatus claim 10; therefore, it is analyzed as previously discussed in claim 10 above.

As to claims 4-5 Olarig (figs. 1- 4) discloses a method, wherein the beacon state is activated by programming a flag bit in a register on the memory module (fig. 6; col. 9, lines 64 through col. 10 line 6).

As to claims 6-9, method claims 6-9 correspond to apparatus claim 10; therefore, they are analyzed as previously discussed in claim 10 above.

Response to Arguments

3. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse, whose telephone number is (571) 272-3813. The examiner can normally be reached on M-F, 8:30-6:00, Alt. Mondays off.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.


Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3824.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Fritz Adlonse

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November 23, 2006


ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100